REMARKS/ARGUMENTS

Claims 1-23 are pending in the present application. Claims 1-5, 7, 8, 12, 14-16 and 19-23 were amended. No claims were added or canceled. Reconsideration of the claims is respectfully requested in view of the above amendments and the following comments.

I. 35 U.S.C. § 112, Second Paragraph: Claims 1-7

The Examiner has rejected claims 1-7 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which applicants regard as the invention.

In rejecting the claims, the Examiner states:

> In claim 1, line 4, "an interrupt" should be change to - the interrupt --. Further, the language: "an interrupt unit control mechanism ... selected type" (lines 3-5) is unclear. Specifically, the step of "determining . . . selected type" is unclear, since the interrupt has already been indicated as "an interrupt of a selected type" (line 3).
>
> Claims 1-7 are directed to an apparatus. However, the essential structural cooperative relationship(s) between the so-called "interrupt unit control mechanism," "interrupt unit," and "performance monitoring unit" have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.
>
> MPEP 2172.01 requires that relationships between elements recited in the claims must be specified. Specifically, MPEP 21 72.02 requires interrelation and structural relationships between essential elements in the claims. Therefore, it is the Examiner's position that the claimed elements, as defined in the originally filed specification and as identified above, are essential elements to the claimed invention. Since they are essential elements as defined in the originally filed specification, their structural cooperative relationships must be provided in the claims. Further, it is also the Examiner's position that the claimed elements, as identified above, function simultaneously, are directly functionally related, directly inter-cooperate, and/or serve independent purposes, as evidenced from the originally filed specification.
>
> If Applicants disagree with the Examiner that the above identified elements, as defined by the originally filed specification, are essential elements to the claimed invention, and that the above identified elements-are directly functionally related, directly inter-cooperate, and/or serve independent purposes, it is requested that Applicants provide evidences showing that the identified elements are not essential elements to the claimed invention, do not function simultaneously, are not directly functionally related, do not directly inter-cooperate, and/or do not serve independent purposes; and state on the record that this is the case.

Office Action dated August 1, 2007, pages 2-3.

By the present Amendment, independent claim 1 and dependent claims 2-5 and 7 have been carefully amended to recite the invention in a clear and definite manner that fully satisfies the requirements of 35 U.S.C. § 112, second paragraph, in all respects. In particular, the claims have been amended to clearly distinguish between an "interrupt" and an "interrupt type" so as to avoid any confusion therebetween. Also, claim 1 has been amended to clearly recite the essential structural cooperative relationship between each of the various components recited therein. Yet further, the claims have been amended to ensure proper antecedent basis for all terminology recited therein.

Applicants respectfully submit that claims 1-7 as presented herein fully satisfy the requirements of 35 U.S.C. § 112, second paragraph, and that the rejection of the claims as being indefinite has been overcome.

II. 35 U.S.C. § 112, First Paragraph: Claims 1-7

The Examiner has rejected claims 1-7 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. This rejection is respectfully traversed.

In rejecting the claims, the Examiner states:

> The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specifically, the language "an interrupt unit control mechanism . . . selected type" (lines 3-5) and "responsive . . . selected type" (lines 9-10) lack clear support from the specification. See also the 35 USC 112, 2"d paragraph. above. It is also noted that Applicants have not pointed out to the originally filed specification by citing page and line number for support of the amendments to claim 1.

Office Action dated August 1, 2007, pages 3-4.

Although Applicants believe the claims do comply with the written description requirements of 35 U.S.C. § 112, first paragraph, in order to expedite prosecution, the claims have been amended to change "interrupt unit control mechanism" to "interrupt unit control register" such that claim 1 now recites "an interrupt unit control register for indicating an interrupt type selected to be monitored". The interrupt unit control register is described, for example, on page 21, lines 26-28 of the specification, as including "a type field that indicates which interrupt type is to generate a performance monitoring counter signal." Further, on page 25, lines 18-20, it is described that the interrupt unit control register is set by supporting software "to indicate which interrupt type is to be monitored."

Applicants respectfully submit that the claims as amended herein fully satisfy the requirements of 35 U.S.C. § 112, first paragraph, in all respects, and that the rejection of claims 1-7 under 35 U.S.C. § 112, first paragraph, has been overcome.

III. 35 U.S.C. § 101: Claims 8-23

The Examiner has rejected claims 8-23 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter. This rejection is respectfully traversed.

In rejecting the claims, the Examiner states:

> With regard to claim 8, a computer program is merely a set of instructions capable of being executed by a computer ("method of executing instructions" as claimed), the computer program itself is not a process, and is a computer program without the computer-readable medium needed to realize the computer program's functionality. Such a computer program is not a process, machine, manufacture or composition of matter.
>
> With regard to claim 16, a computer program is merely a set of instructions capable of being executed by a computer, the computer program itself is not a process, and is a computer program without the computer-readable medium needed to realize the computer program's functionality. Such a computer program is not a process, machine, manufacture or composition of matter. A computer program/instructions must be stored in a computer readable medium and executed by a machine to perform a task. As claimed, the computer "instructions" are neither stored or are executed. Further, as disclosed in the specification, the computer readable medium can be an "digital and analog communication links, wired or wireless communications links using transmission forms, such as, for example, radio frequency and light wave transmissions." It is clear that "radio frequency and light wave transmissions" may transmit but simply cannot store and record any instruction; and are not a tangible media.
>
> With regard to claim 23, a computer program is merely a set of instructions capable of being executed by a computer ("computer implemented method" as claimed), the computer program itself is not a process, and is a computer program without the computer-readable medium needed to realize the computer program's functionality. Such a computer program is not a process, machine, manufacture or composition of matter.

Office Action dated August 1, 2007, pages 4-5.

By the present Amendment, method claim 8 has been amended to recite "[a] method of executing instructions in a data processing system, comprising:..." In addition, claim 16 has been amended to recite "[a] computer program product stored in a computer readable medium in a data processing system for processing instructions..." Also, claim 23 has been amended to recite "[a] A computer implemented method for executing instructions stored in a computer readable medium..."

Applicants respectfully submit that claims 8, 16 and 23 as amended herein fully satisfy the requirements of 35 U.S.C. § 101, and that the rejection of claims 8-23 under 35 U.S.C. § 101 has been overcome.

Further, it is noted that claim 23 has been rejected only under 35 U.S.C. § 101. In view of the above amendments to that claim, claim 23 should now be allowed and it is respectfully requested that the Examiner so find.

IV. 35 U.S.C. § 102, Anticipation: Claims 1-6, 8-12, and 16-21

The Examiner has rejected claims 1-6, 8-12, and 16-21 under 35 U.S.C. § 102(b) as being anticipated by Levine et al., U.S. Patent No. 5,691,920 (hereinafter "Levine"). This rejection is respectfully traversed.

In rejecting the claims, the Examiner states:

> Referring to claim 1:
>
> Levine discloses a performance-monitoring unit (Abstract) and one or more hardware counters (column 10, lines 58-59) located within the performance-monitoring unit (figure 4, structures 50 and 51). Levine discloses a variety of operations of the performance-monitoring unit (column 10, lines 34-56); Levine discloses setting the performance-monitoring unit to selectively monitor the instructions within specific addresses (column 12, 2nd paragraph). The instructions within specific addresses are a selected interrupt handling routine, and the Levine's selective monitoring on the particular instructions is the claimed hardware counters' counting the occurrence of events during an interrupt of a selected type. Furthermore, Levine disclosed two separate counters for selected events (figure 6A, column 8, lines 57-60). With regard to the newly added limitations to claim 1 by the RCE filed 6/11/2007, it is clear that in Levine, at least bits 5 and 16 in a register field of a particular MMCR associated with a particular counter PMC indicate "an interrupt of a selected type" or specifically, the performance monitoring interrupt type. In other words, the type of interrupt indicated and associated with MMCR shown below is the performance monitoring interrupt type.

BITS 0-4 COUNTING ENABLES	BIT 5 INTERRUPT ENABLE	BITS 6-15	BIT 16 PMC1 INTERRUPT CONTROL	BIT 17 PMCn, n>1 COUNT CONTROL	BIT 18 PMCn, n>1 COUNT CONTROL	BITS 19-25 PMC1 EVENT SELECTION	BITS 26-31 PMC2 EVENT SELECTION

MONITOR MODE CONTROL REGISTER 0 (MMCR0)

FIGURE 6A

Further, it is also clear the performance monitoring interrupt is presented to the interrupt resolution logic or interrupt handler 57, which uses a plurality of interrupt handling routines to serve the interrupts depending from the types of

> interrupts. In other words, depending on a particular type of interrupt, the interrupt handler 57 will select a particular interrupt handling routine among the plurality of interrupt handling routines employed by the interrupt handler 57. It is clear that the interrupt handler 57 MUST be able to determine which type of interrupt presented to it before it selects the corresponding interrupt handling routine accordingly. In the instant case, the interrupt handler 57 must be able to determine that the presented interrupt is the performance monitoring interrupt before it selects a routine designed for performance monitoring. Thus, it is clear that the interrupt resolution logic or interrupt handler 57 is readable as the "interrupt unit."

Office Action dated August 1, 2007, pages 6-7.

Claim 1 as amended herein is as follows:

> 1. A data processing system for qualifying events when an interrupt occurs, comprising:
>
> an interrupt unit control register for indicating an interrupt type selected to be monitored;
>
> an interrupt unit, responsive to an interrupt occurring during code execution, for determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register;
>
> a performance monitoring unit; and
>
> one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). In this case each and every feature of the presently claimed invention is not identically shown in the cited reference, arranged as they are in the claims. With respect to claim 1, in particular, Levine does not disclose or suggest "an interrupt unit control register for indicating an interrupt type selected to be monitored", "an interrupt unit, responsive to an interrupt occurring during code execution, for determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register", or "one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register."

Initially, Levine does not disclose or in any way suggest "an interrupt unit control register for indicating an interrupt type selected to be monitored" as presently recited in claim 1. Levine does not describe interrupt types and does not disclose a register that indicates an interrupt type selected to be monitored. Bits 5 and 16 illustrated in Figure 6A of Levine reproduced by the Examiner are not interrupt types selected to be monitored, but, at best, may relate to states of an interrupt.

Furthermore, Levine does not disclose "an interrupt unit, responsive to an interrupt occurring during code execution, for determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register" as now recited in claim 1. In rejecting the claims, the Examiner construes the interrupt handler 57 in Levine as corresponding to the interrupt unit recited in claim 1. In particular, the Examiner points out that interrupt handler 57 in Levine selects one of interrupt handling routines 71, 77 and 79 illustrated in Figure 4, and concludes "[i]t is clear that the interrupt handler 57 MUST be able to determine which type of interrupt presented to it before it selects the corresponding interrupt handling routine accordingly." Applicants respectfully disagree.

Applicants respectfully submit that Levine nowhere discloses or suggests that interrupt handler 57 selects one or another of interrupt handling routines 71, 77 and 79 based on interrupt type, and Levine certainly does not disclose that interrupt handler 57 selects a particular interrupt handling routine based on an interrupt type selected to be monitored. Neither the Monitor Mode Control Register illustrated in Figure 6A referred to by the Examiner nor the discussion of the interrupt handling routines in column 9, lines 46-62 in Levine suggests that interrupt handler 57 selects a particular interrupt routine based on interrupt type. Levine does not disclose that interrupt handler 57 functions to be "responsive to an interrupt occurring during code execution for determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register" as now recited in claim 1.

Levine also does not disclose or suggest "one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register." Although Levine may disclose counters in performance monitor 50 illustrated in Figure 4 of Levine, the counters are described as being for counting "processor/storage related events" (see col. 8, lines 33-41 of Levine). Levine does not disclose that the counters count events that occur during processing of an interrupt "responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register" as required in claim 1. Levine does not disclose interrupt types and does not determine if an interrupt that occurs during code execution is of an interrupt type selected to be monitored.

For at least all the above reasons, Levine does not identically show every element recited in claim 1 arranged as they are in the claim, and does not anticipate claim 1.

Claims 2-6 depend from and further restrict claim 1, and are also not anticipated by Levine, at least by virtue of their dependency. Furthermore, many of these claims recite additional features that are not disclosed or suggested by Levine. For example, claim 5 depends from claim 1 and recites that the one or more hardware counters count events that occur during processing of the interrupt based on the interrupt type of the interrupt. Since, as indicated above, Levine does not disclose different interrupt types, Levine also does not disclose counting events during an interrupt according to the interrupt type of the interrupt. Claim 5, accordingly, patentably distinguishes over Levine in it own right as well as by virtue of its dependency.

Independent claim 8, as amended herein is as follows:

> 8. A method of executing instructions in a data processing system, comprising:
> receiving a signal at a microprocessor of the data processing system for invoking an interrupt, wherein the invoked interrupt includes a plurality of states; and
> counting at least one event for a selected state of the plurality of states during processing of the invoked interrupt.

In rejecting claim 8, the Examiner states:

> Referring to claims 8-10: It is clear that the states of the performance monitor interrupt include at least the state wherein an interrupt signal is generated, and a state wherein the interrupt is serviced or processed. As discussed above, during servicing or processing the performance monitor interrupt, multiple events are counted by hardware counters located inside the performance monitor unit 50. The counters count the occurrence of events during the interrupt service routine, which is a "state" of the performance monitor interrupt.

Office Action dated August 1, 2007, page 8.

The Examiner construes interrupt states as including a state when an interrupt signal is generated, and a state when the interrupt is serviced, and thus concludes that Levine discloses a plurality of interrupt states. As amended, however, claim 8 clarifies that the invoked interrupt includes a plurality of interrupt states, and that at least one event for a selected state is counted during processing of the invoked interrupt. Levine does not disclose an invoked interrupt that includes a plurality of states, and also does not disclose counting at least one event for a selected state of the plurality of states during processing of the invoked interrupt.

Claim 8, accordingly, is also not anticipated by Levine and patentably distinguishes over Levine in its present form.

Independent claim 16 recites similar subject matter as claim 8, and is also not anticipated by Levine for similar reasons as claim 8. Claims 9-12 and 17-21 depend from and further restrict one of claims 8 and 16 and are also not anticipated by Levine.

Therefore, the rejection of claims 1-6, 8-12, and 16-21 under 35 U.S.C. § 102(b) has been overcome.

V. 35 U.S.C. § 103, Obviousness: Claims 1-6, 8-14, and 16-21

The Examiner has rejected claims 1-6, 8-14, and 16-21 under 35 U.S.C. § 103(a) as being unpatentable over the admitted prior art in view of Levine. This rejection is respectfully traversed.

In rejecting the claims, the Examiner states:

> Referring to claim 1: The admitted prior art discloses a performance-monitoring unit (Specification, page 3, last paragraph, line 6) and one or more hardware counters (Specification, page 3, last paragraph, lines 1-2) located within the performance-monitoring unit. The admitted prior art does not disclose that the one or more hardware counters count the occurrence of events during an interrupt of a selected type.
>
> Levine discloses a variety of operations of the performance-monitoring unit (column 10, lines 34-39); Levine discloses setting the performance-monitoring unit to selectively monitor the instructions within specific addresses (column 12, 2"d paragraph). The instructions within specific addresses are a selected interrupt handling routine, and the Levine's selective monitoring on the particular instructions is the claimed hardware counters' counting the occurrence of events during an interrupt of a selected type. Levine teaches one to analyze the system performance and to focus particular sets of instructions for examining the performance bottleneck. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Levine's teaching onto the admitted prior art because Levine teaches one to analyze the system performance and to focus particular sets of instructions for examining the performance bottleneck.

Office Action dated August 1, 2007, pages 10-11.

The Examiner bears the burden of establishing a *prima facie* case of obviousness based on the prior art when rejecting claims under 35 U.S.C. §103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). Additionally, all limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Therefore, no *prima facie* obviousness rejection can be established if the proposed combination does not teach all of the features of the claimed invention. Furthermore, if an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

In the present case, neither the admitted prior art nor Levine nor their combination discloses or suggests "an interrupt unit control register for indicating an interrupt type selected to be monitored", "an interrupt unit, responsive to an interrupt occurring during code execution, for determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register", or "one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register" as recited in claim 1. Levine does not disclose the subject matter of claim 1 for reasons discussed in detail above. The admitted prior art is cited as disclosing a performance monitoring unit having hardware counters, and does not supply the deficiencies in Levine. Accordingly, the references do not teach all of the features of the claimed invention as recited in claim 1, and the Examiner has, thus, not established a *prima facie* case of obviousness in rejecting claim 1.

For similar reasons as discussed above, the admitted prior art in view of Levine also does not teach all of the features of the claimed invention as recited in claims 8 and 16, and the Examiner has also not established a *prima facie* case of obviousness in rejecting claims 8 and 16 as well.

Claims 1-6, 8-14 and 16-21 are, therefore, not obvious in view of the admitted prior art and Levine, and are allowable thereover in their present form.

Therefore, the rejection of claims 1-6, 8-14, and 16-21 under 35 U.S.C. § 103(a) has been overcome.

VI. 35 U.S.C. § 103, Obviousness: Claims 7, 15 and 22

The Examiner has rejected claims 7, 15, and 22 under 35 U.S.C. § 103(a) as being unpatentable over Levine in view of previously cited "Computer System Architecture" by Morris Mano or as being unpatentable over the admitted prior art in view of Levine and Mano. These rejections are respectfully traversed.

In rejecting the claims, the Examiner states:

> Referring to claims 7, 15, and 22: The disclosures of the admitted prior art and Levine are stated above. As stated above, Levine discloses monitoring the particular interrupt according to the instructions address, and Levine discloses two separate counters for event selections (figure 6A, column 8, lines 57-60); thus, Levine discloses the hardware counters counting events separately. But neither explicitly discloses a second interrupt interrupts a first interrupt.
>
> Mano, as a popular academic textbook, discloses managing interrupt according to its priority (pages 434-435). Mano discloses that a higher priority interrupt can interrupt an in-process lower priority interrupt (page 435, 2nd

> paragraph). Mano teaches one to manage the limited system resources by prioritizing interrupt. Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Mano's teaching onto the admitted prior art and Levine because Mano teaches one to manage the limited system resources by prioritizing interrupt.

Office Action dated August 1, 2007, pages 14-15.

Claims 7, 15 and 22 depend from and further restrict one of independent claims 1, 8 and 16. Mano does not supply the deficiencies in Levine or in the admitted prior art in view of Levine as discussed above. Claims 7, 15 and 22, accordingly, are allowable in their present form by virtue of their dependency.

In addition, although Mano may disclose monitoring interrupts according to their priority, the reference does not disclose or suggest "a second interrupt that interrupts the first interrupt, wherein the one or more hardware counters separately count the events that occur during the processing of the first interrupt and events that occur during processing of the second interrupt" as more clearly recited in amended claim 7 and corresponding claims 15 and 22. As pointed out above, although Levine may disclose counters in performance monitor 50 illustrated in Figure 4 of Levine, the counters are described as being for counting "processor/storage related events", and Levine also does not disclose hardware counters that separately count events that occur during the processing of the first interrupt and events that occur during processing of the second interrupt" as recited in claims 7, 15 and 22. Accordingly, claims 7, 15 and 22 are also allowable in their own right as well as by virtue of their dependency.

Therefore, the rejection of claims 7, 15, and 22 under 35 U.S.C. § 103(a) has been overcome.

VII. Conclusion

It is respectfully urged that claims 1-23 patentably distinguish over the cited art and that this application is now in condition for allowance. It is, accordingly, respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: November 1, 2007

Respectfully submitted,

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